

FIG. 1a Deposition of first electrode layer

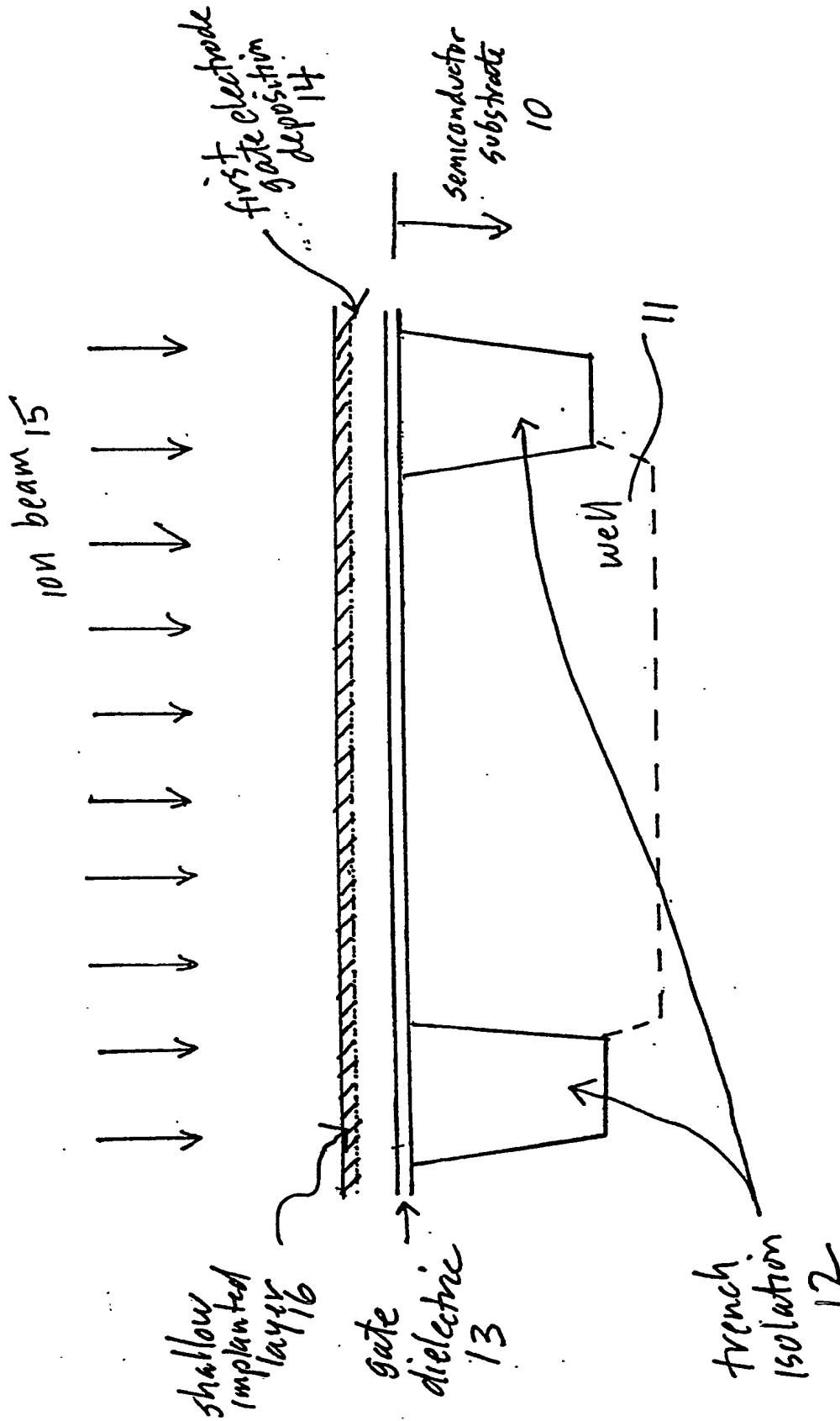


FIG 1B Process through first ion implant

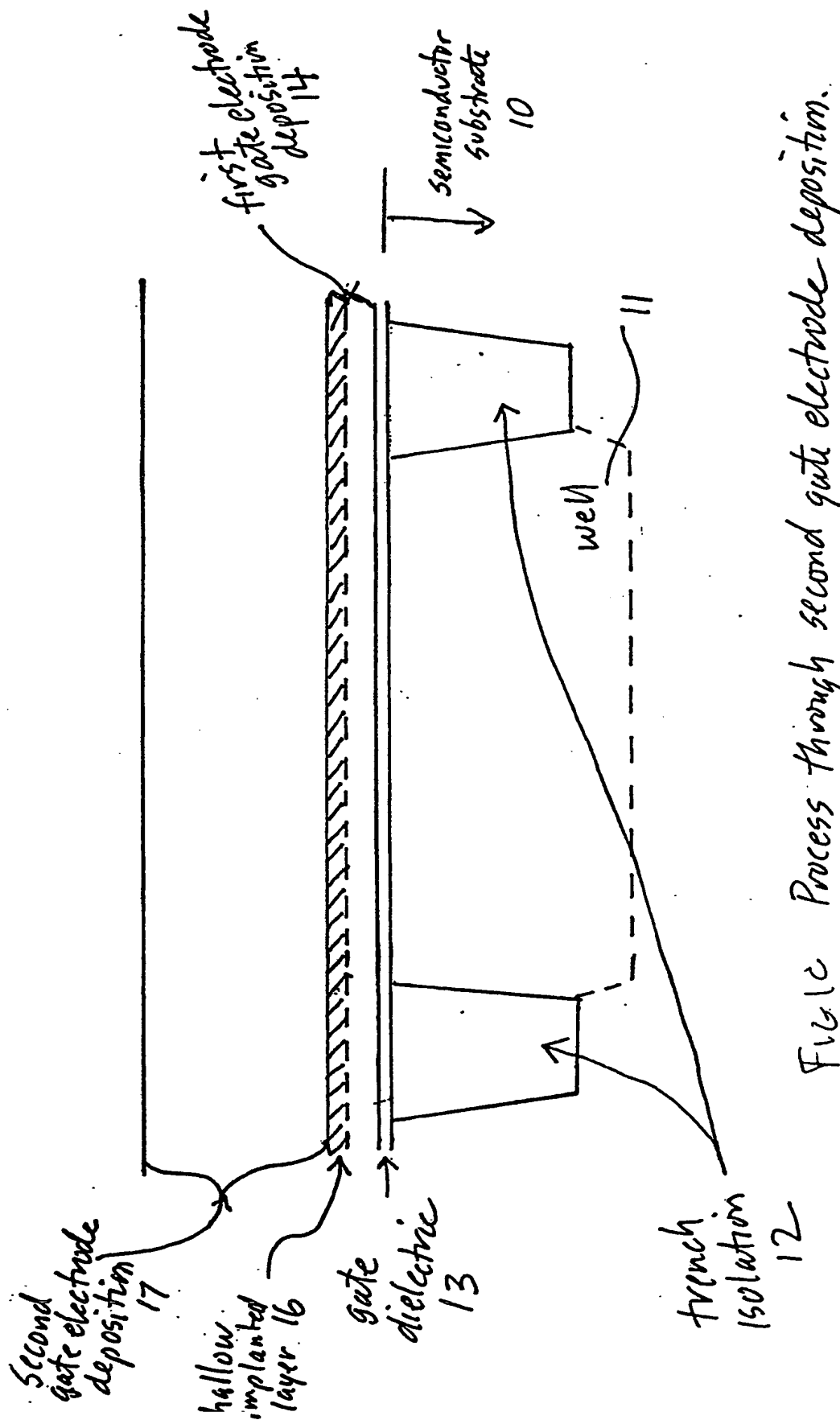


FIG 1C Process through second gate electrode deposition.

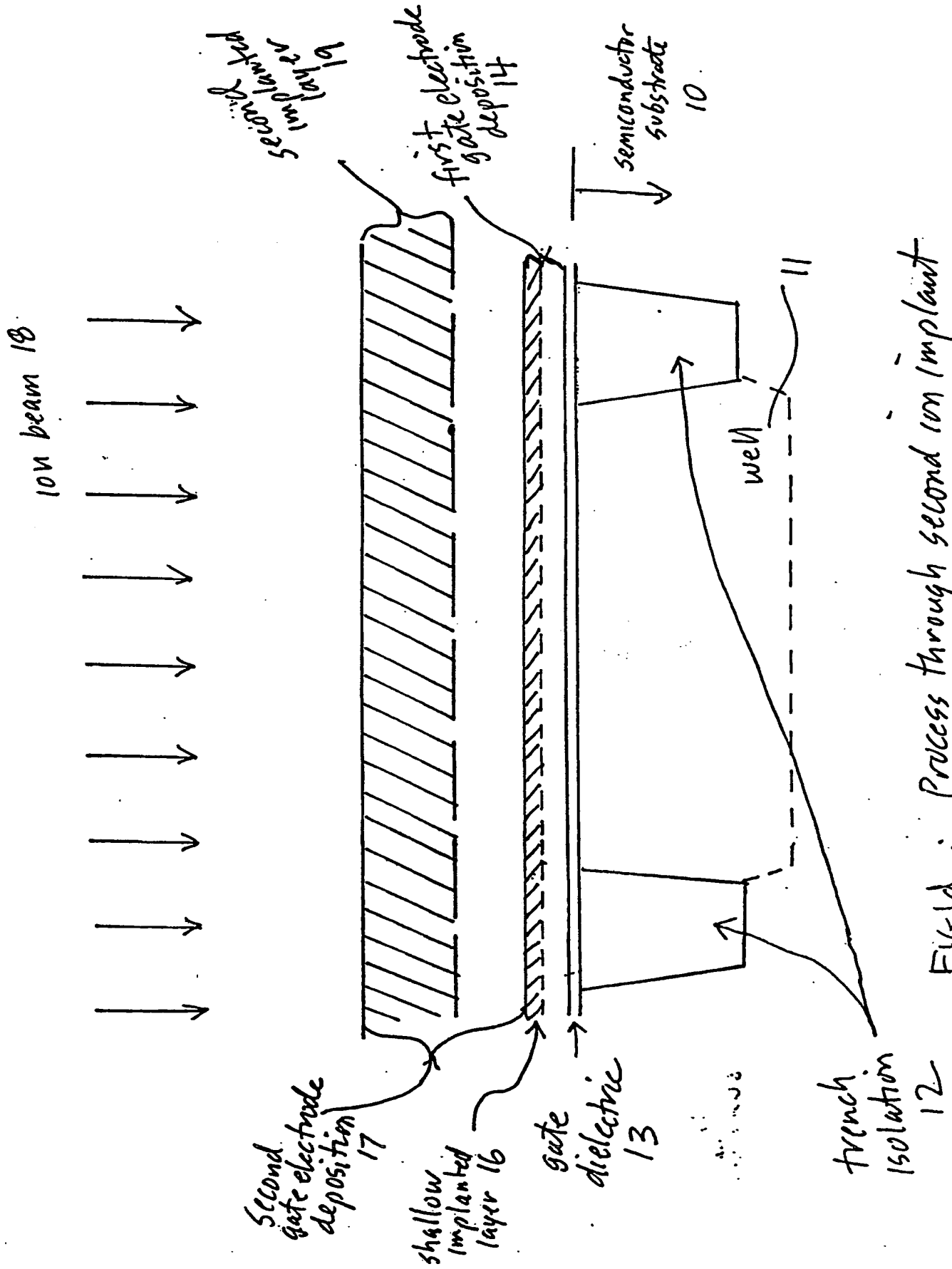


FIG 1d : Process through second ion implant

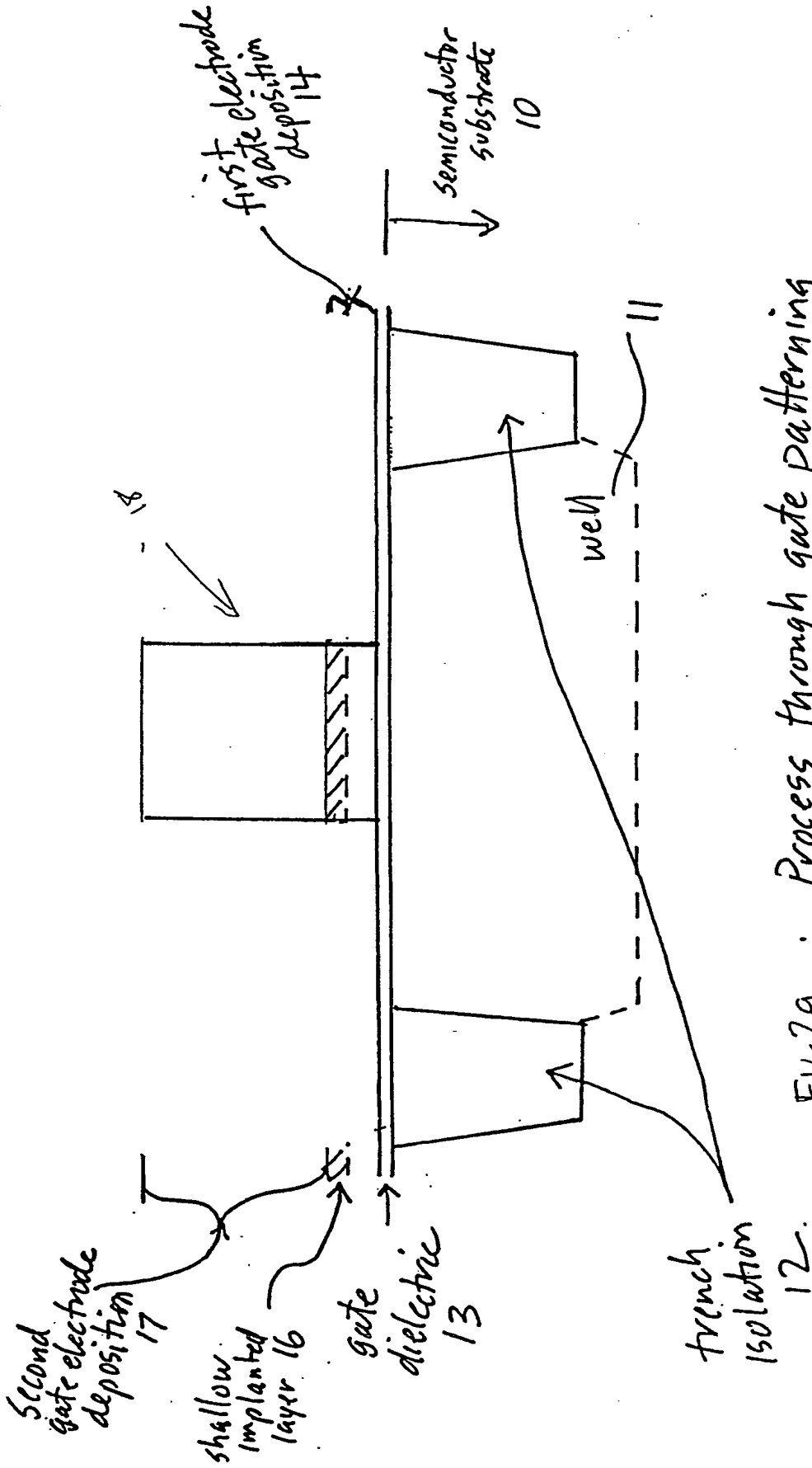


FIG 29 :: Process through gate patterning

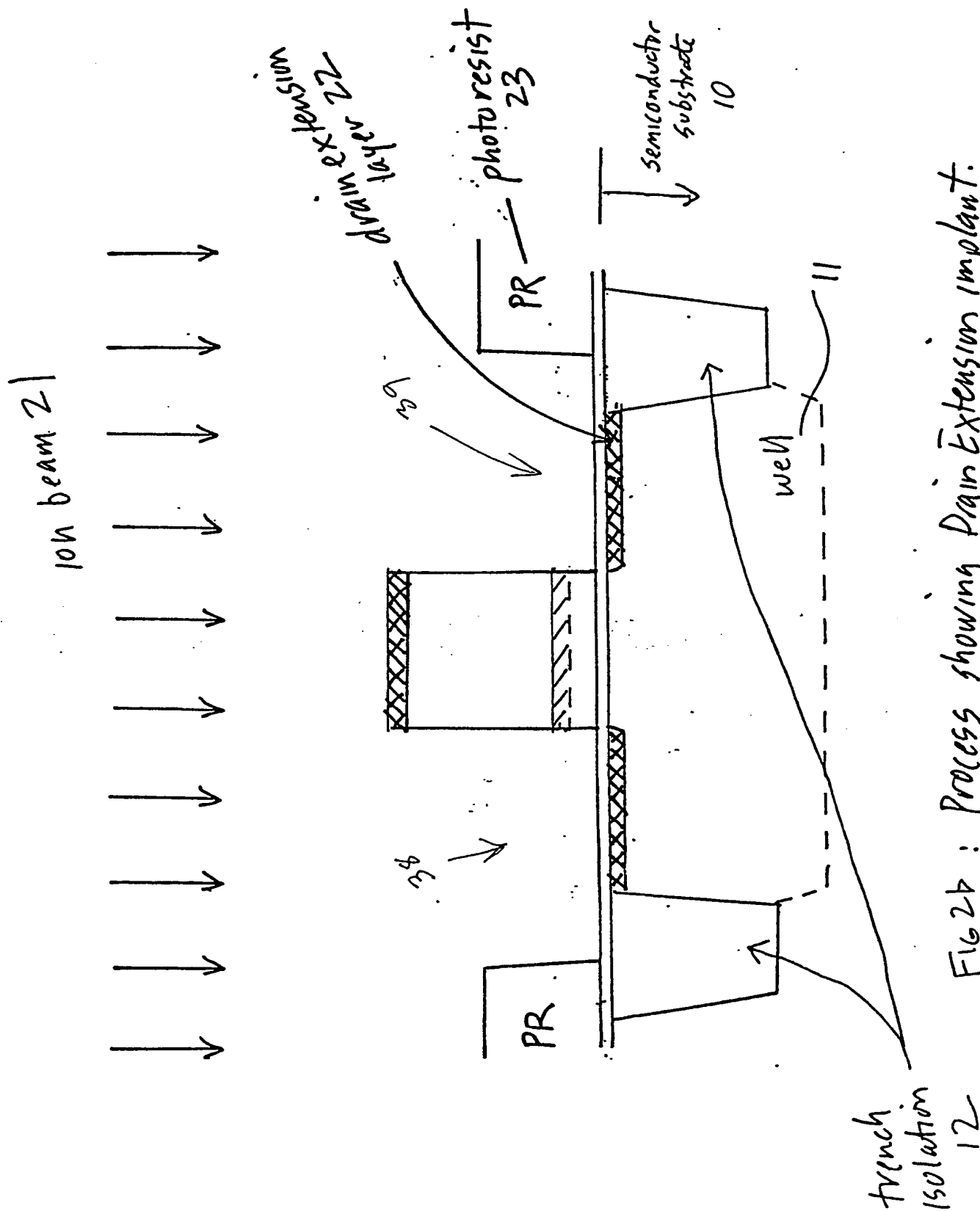


FIG 2b : Process showing Drain Extension implant.

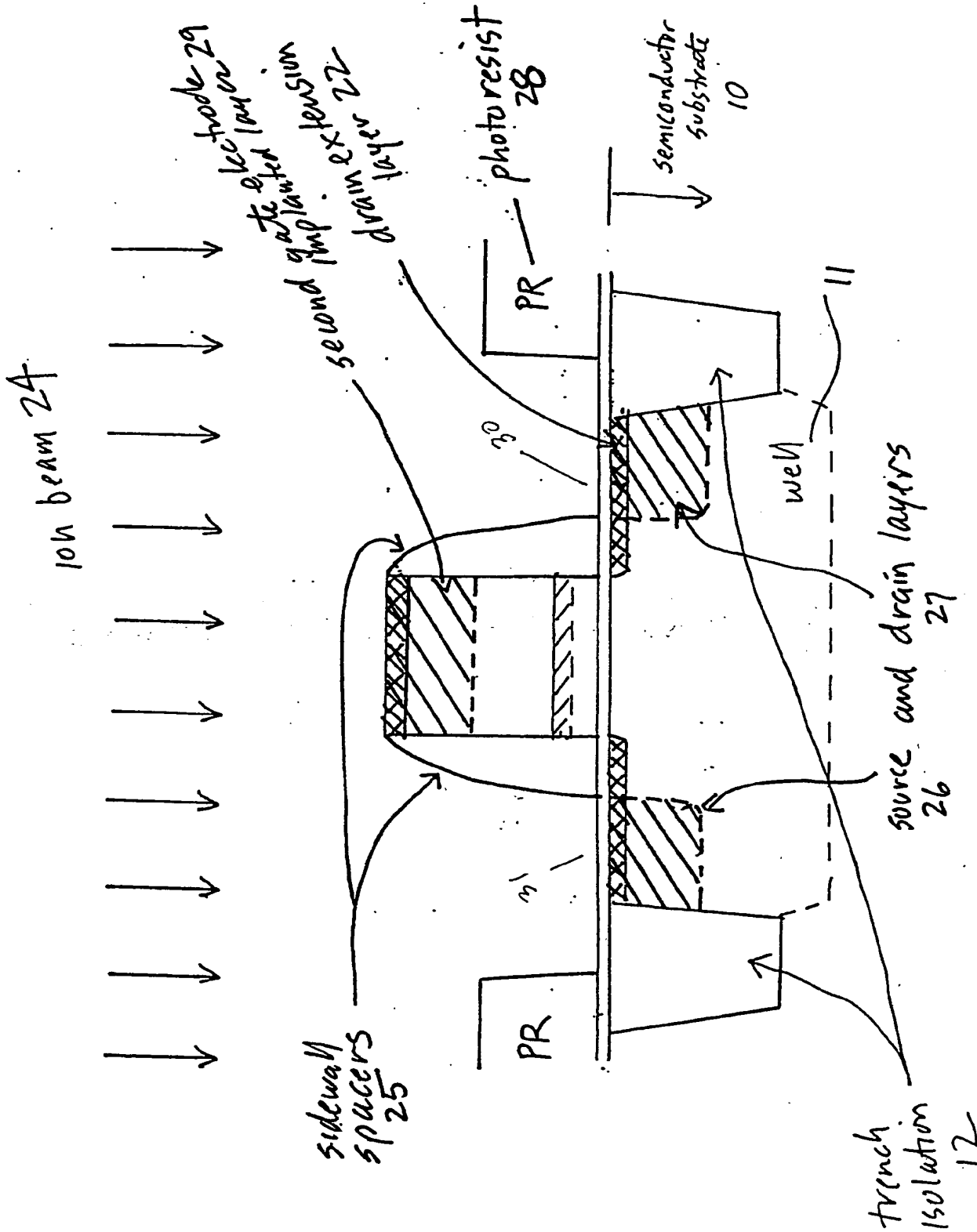


FIG. 2c Process showing source and drain implant providing gate electrode second implant doping.

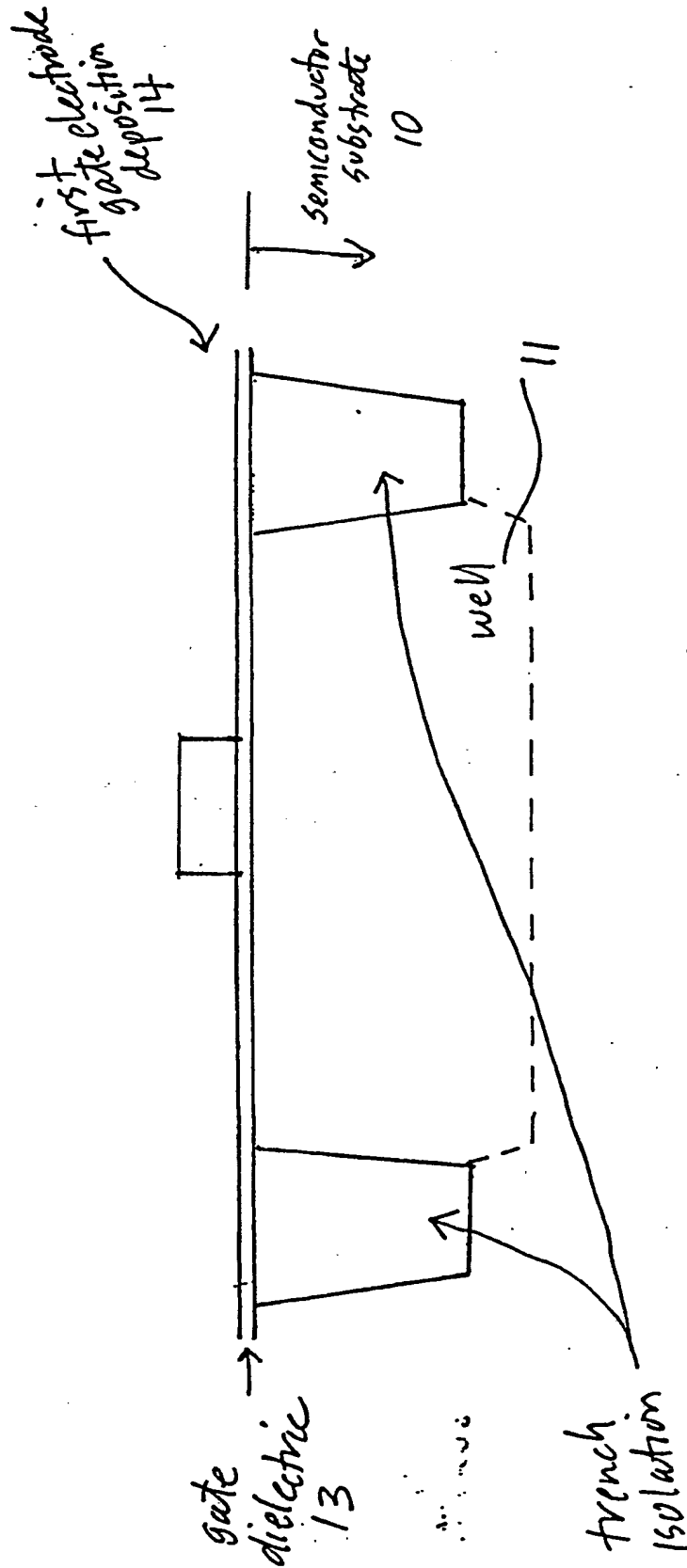


FIG 3a Process through patterning of the first gate electrode

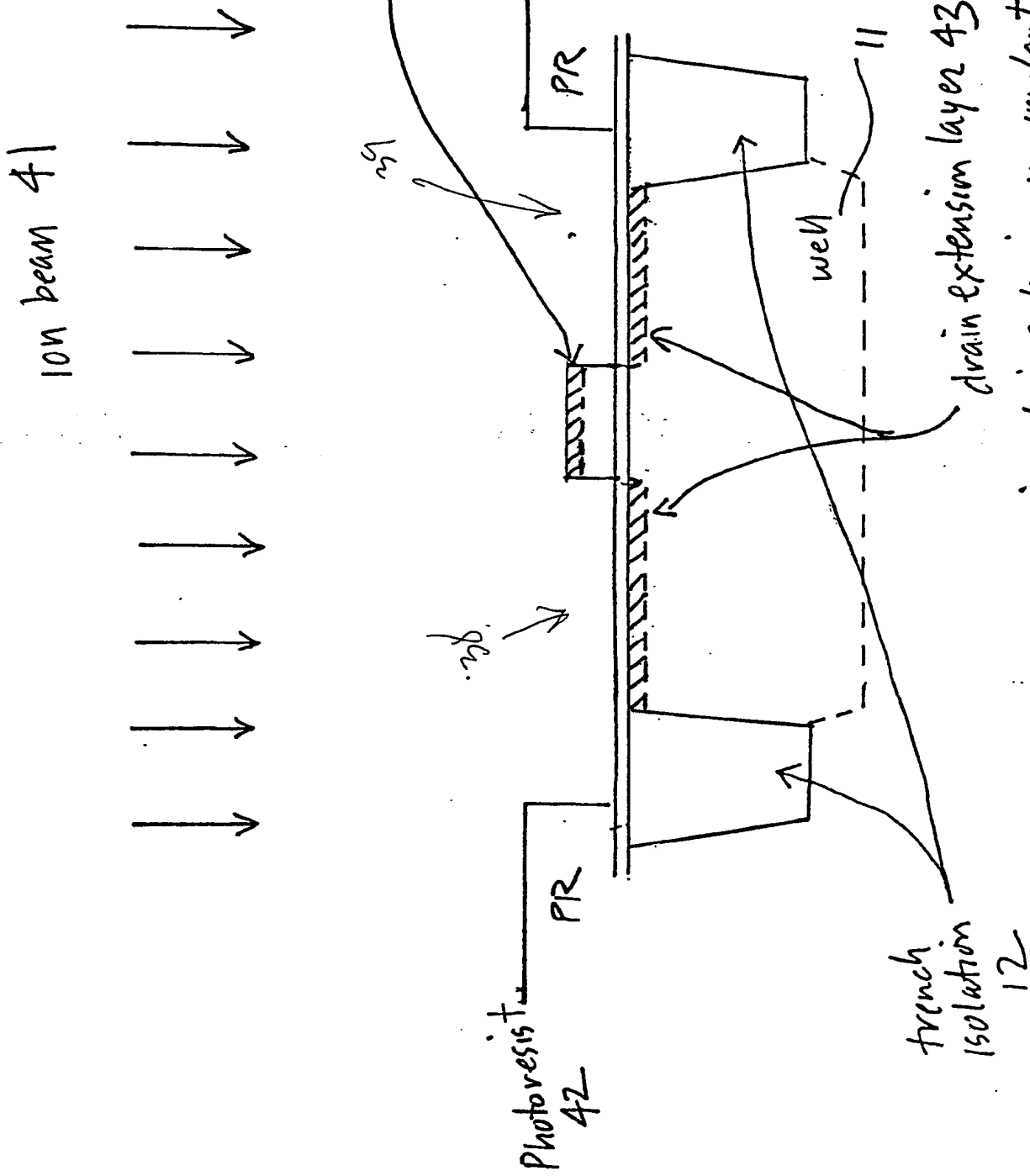


FIG 3P : Process showing drain extension ion implant also forming first (shallow) gate electrode implanted layer.

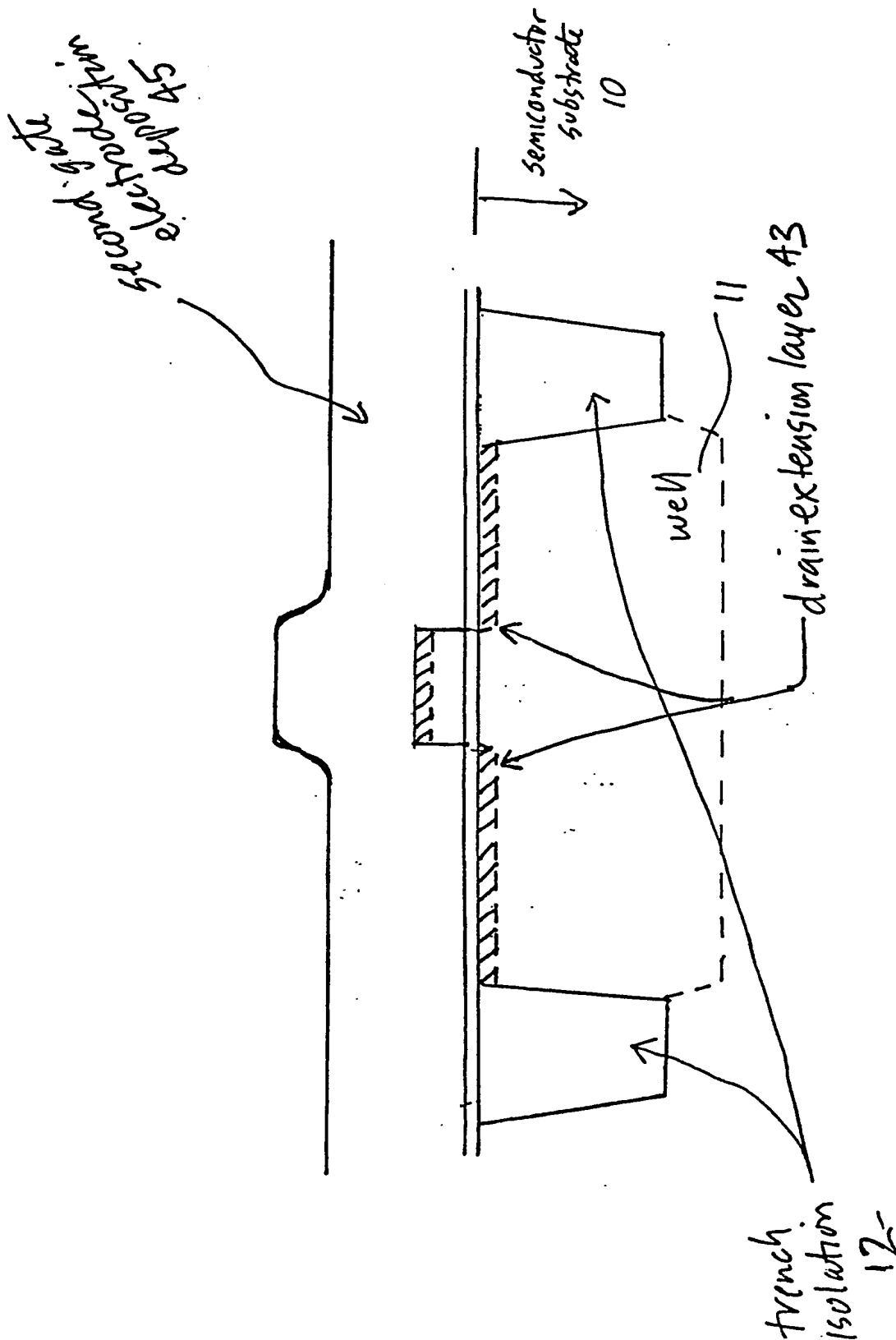


FIG 3C : Second gate electrode deposition

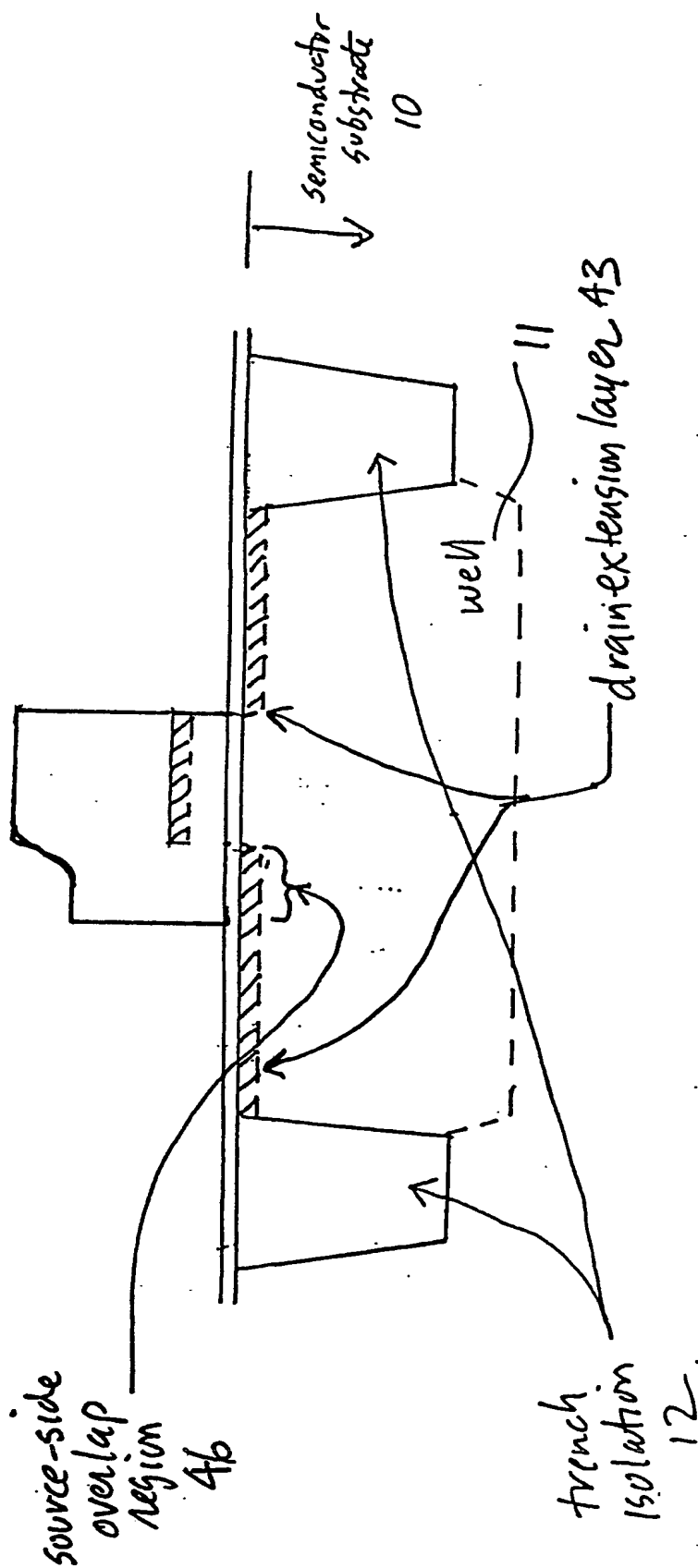


FIG 3d Process showing gate electrode patterning results.

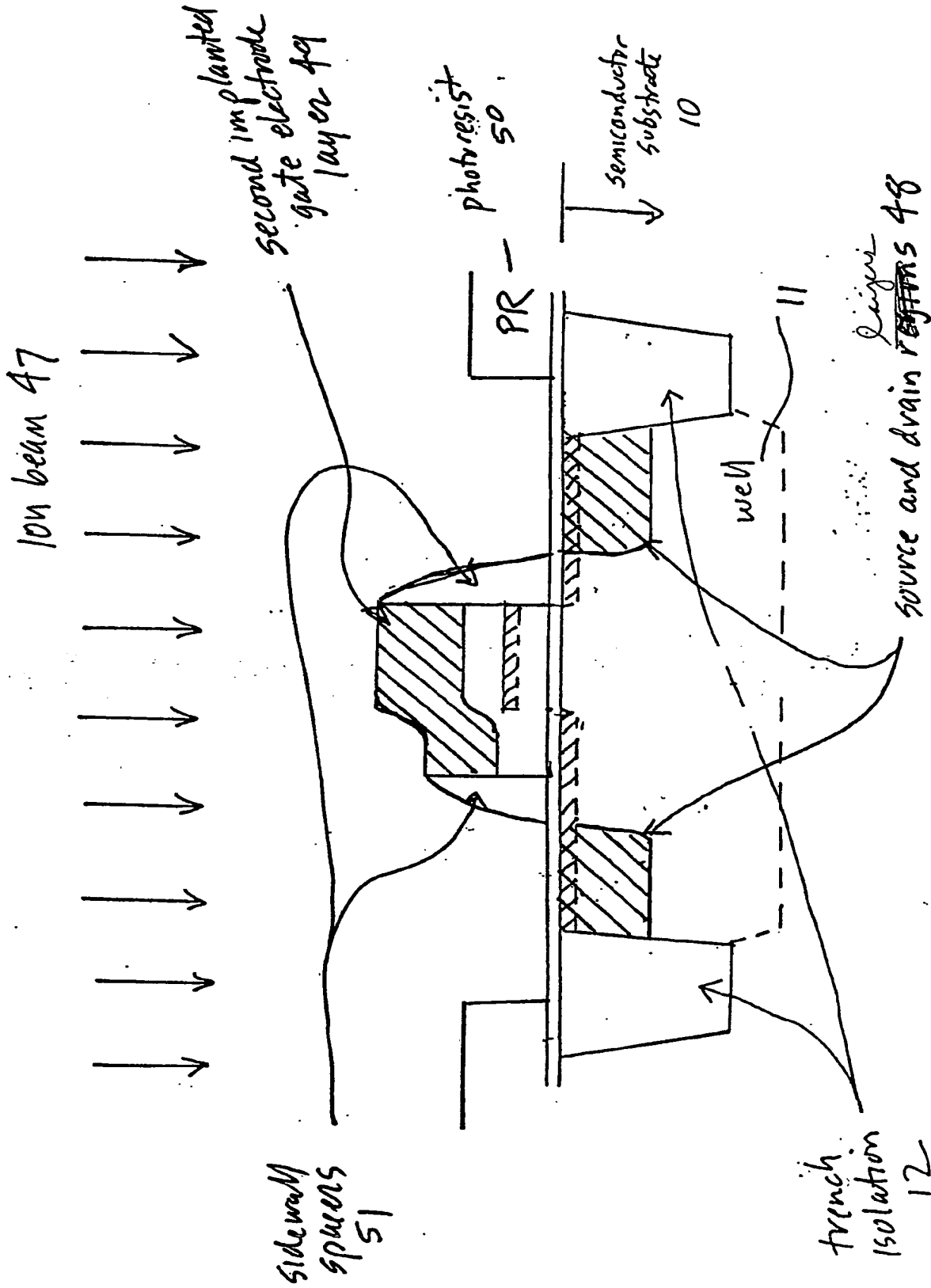


FIG 3e Second ion implant forms source and drain and second gate electrode implanted layer.

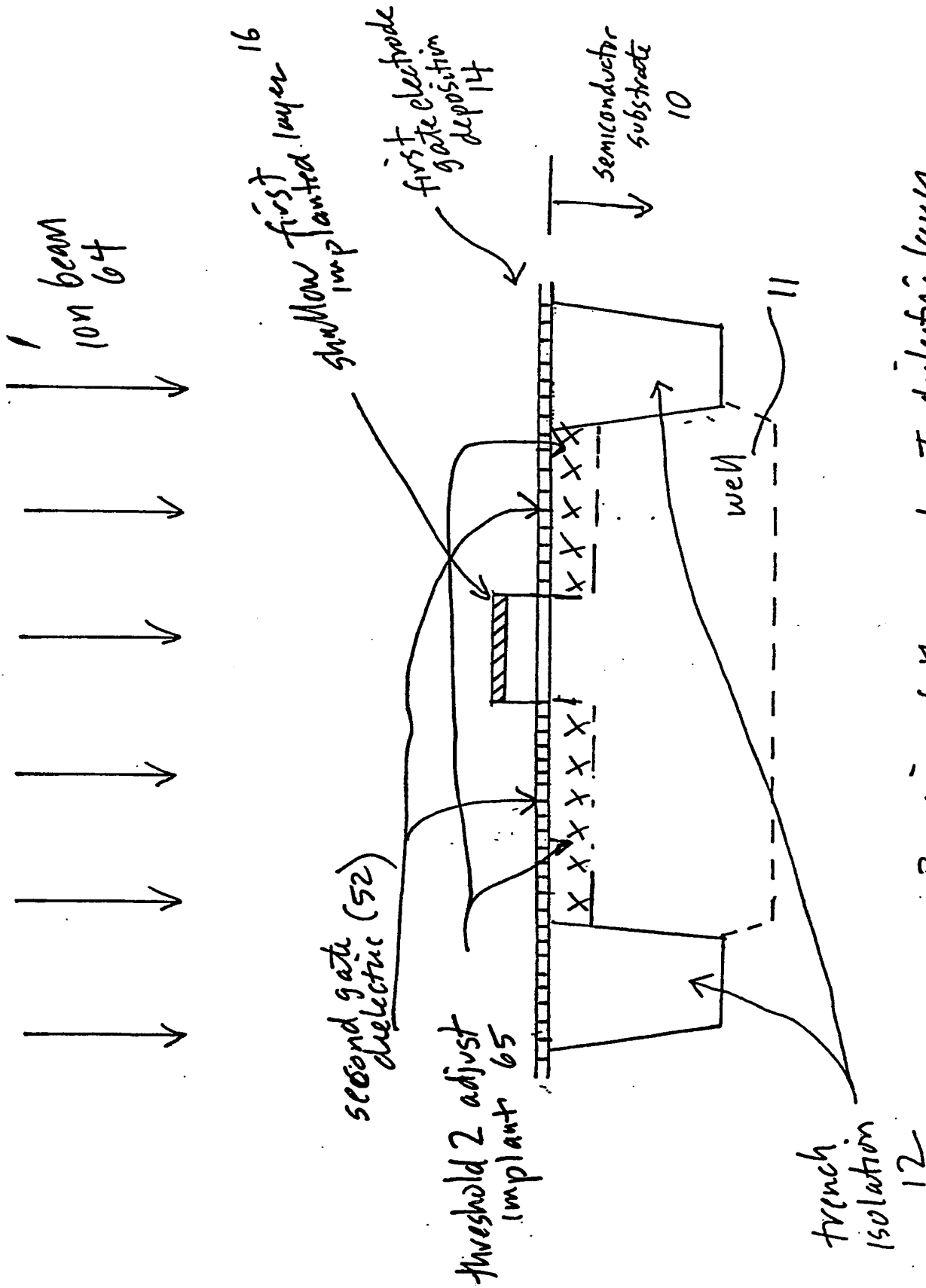


Fig 4a : Processing of the second gate dielectric layer.

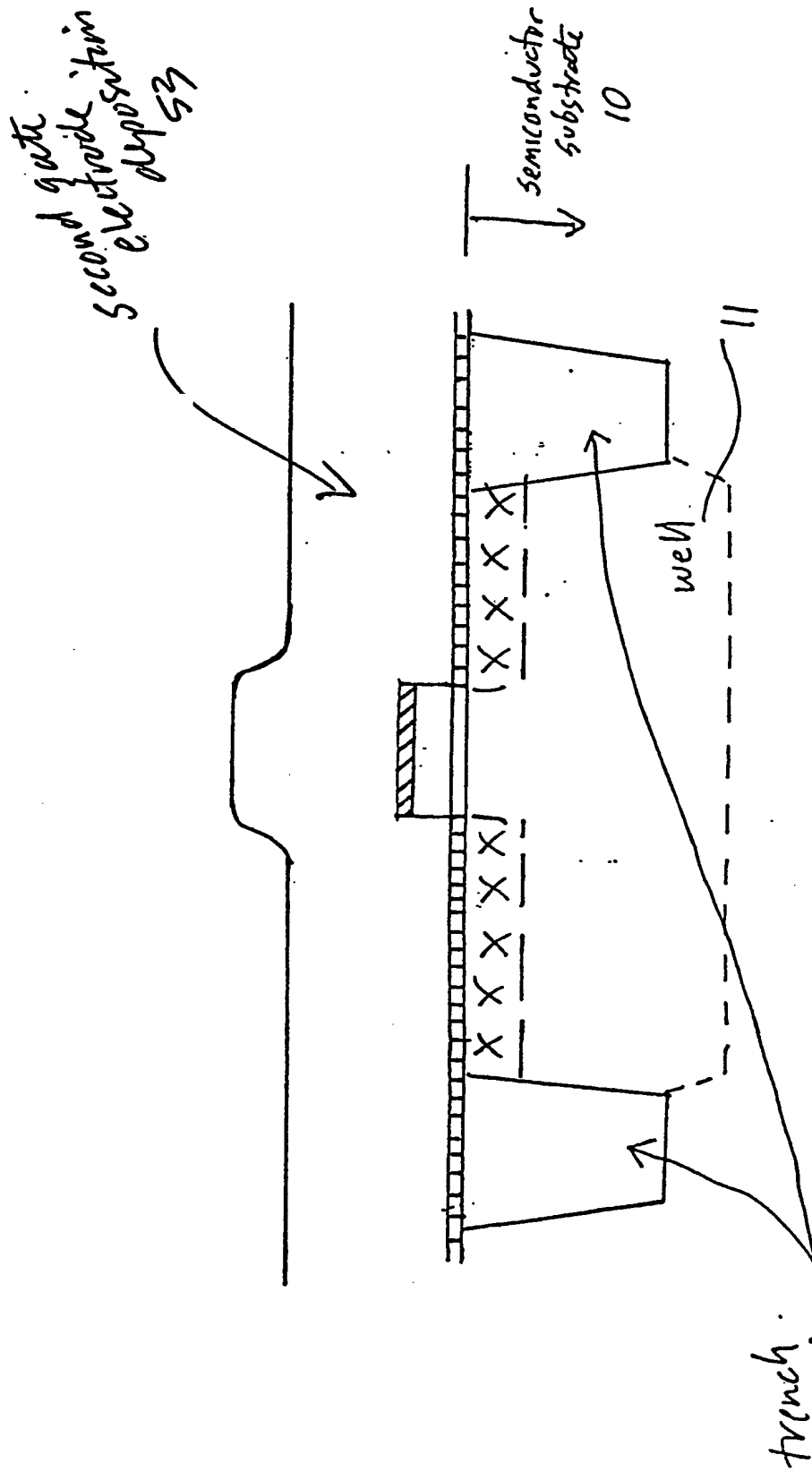


FIG 4B Deposition of second gate electrode layer.

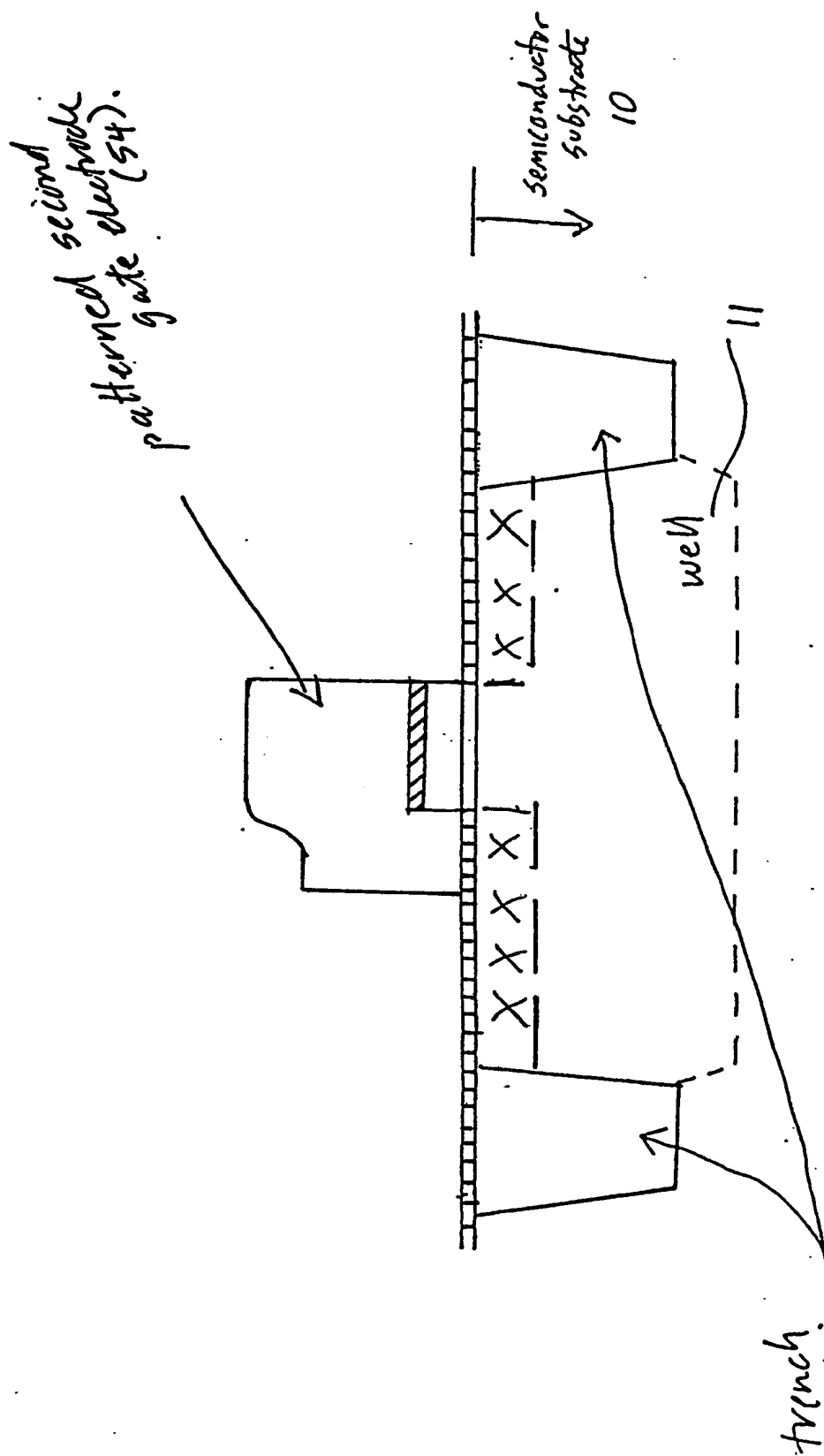


FIG 4c Patterning of second gate electrode.

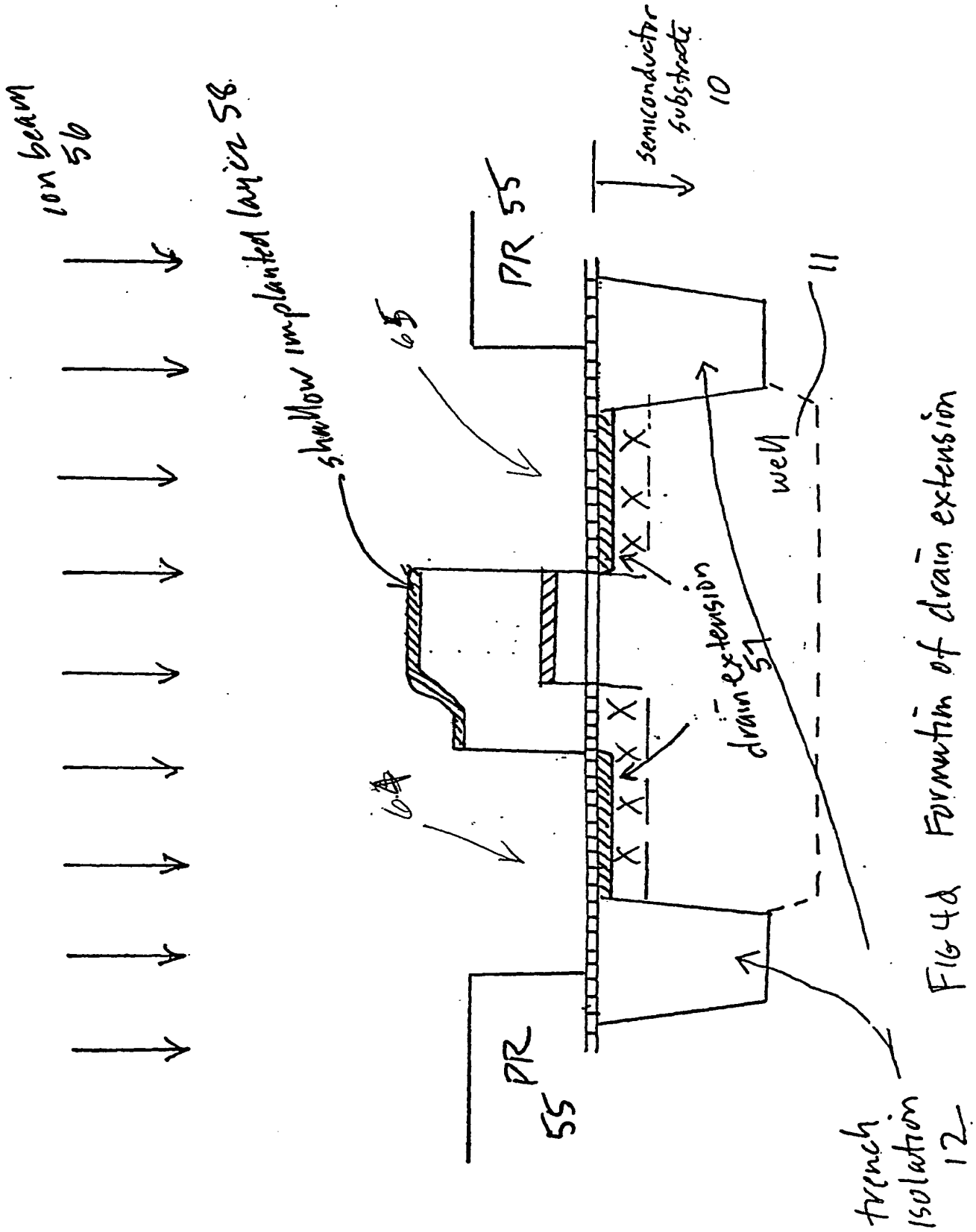


FIG 4d Formation of drain extension

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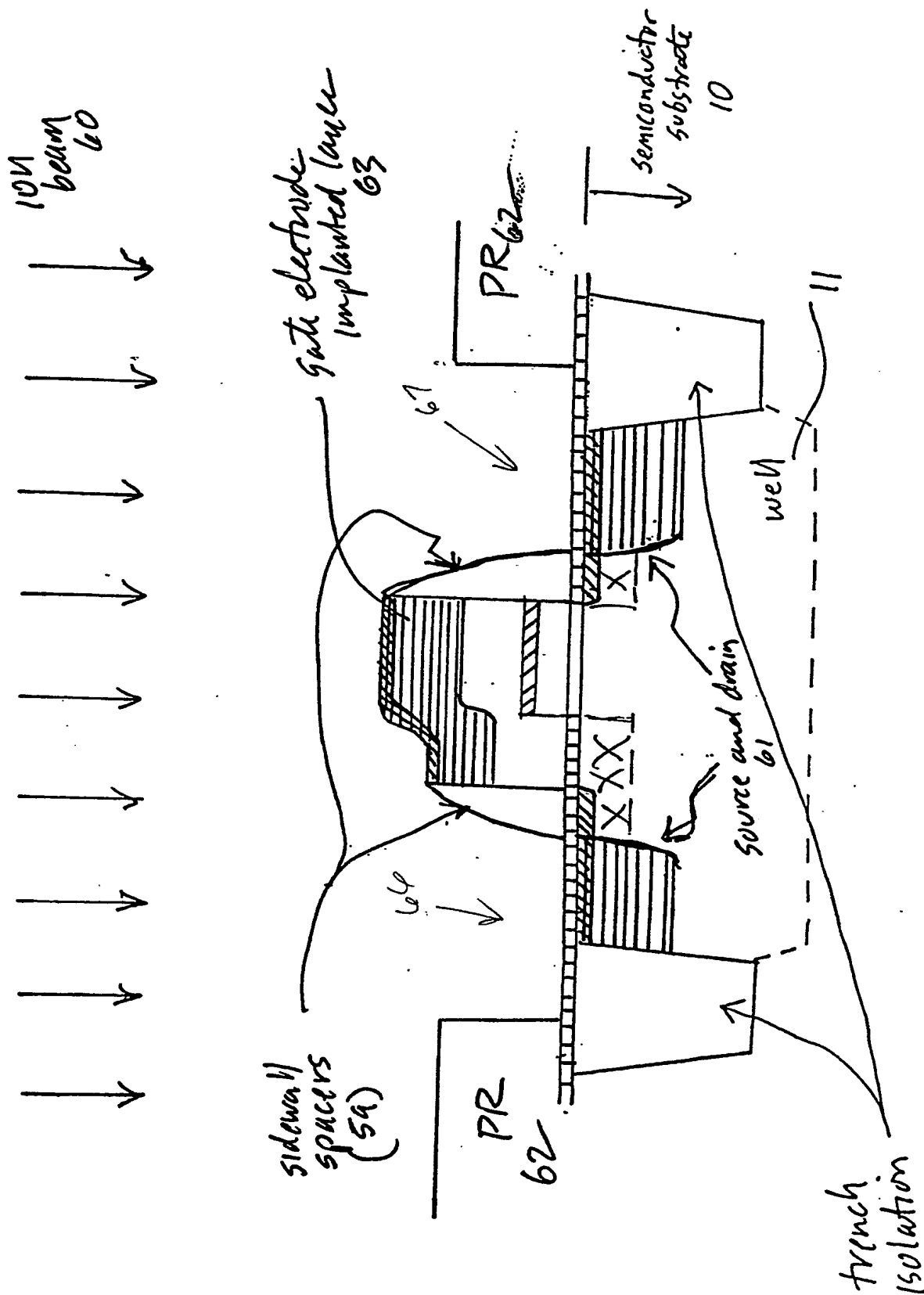


FIG 4e Formation of source and drain

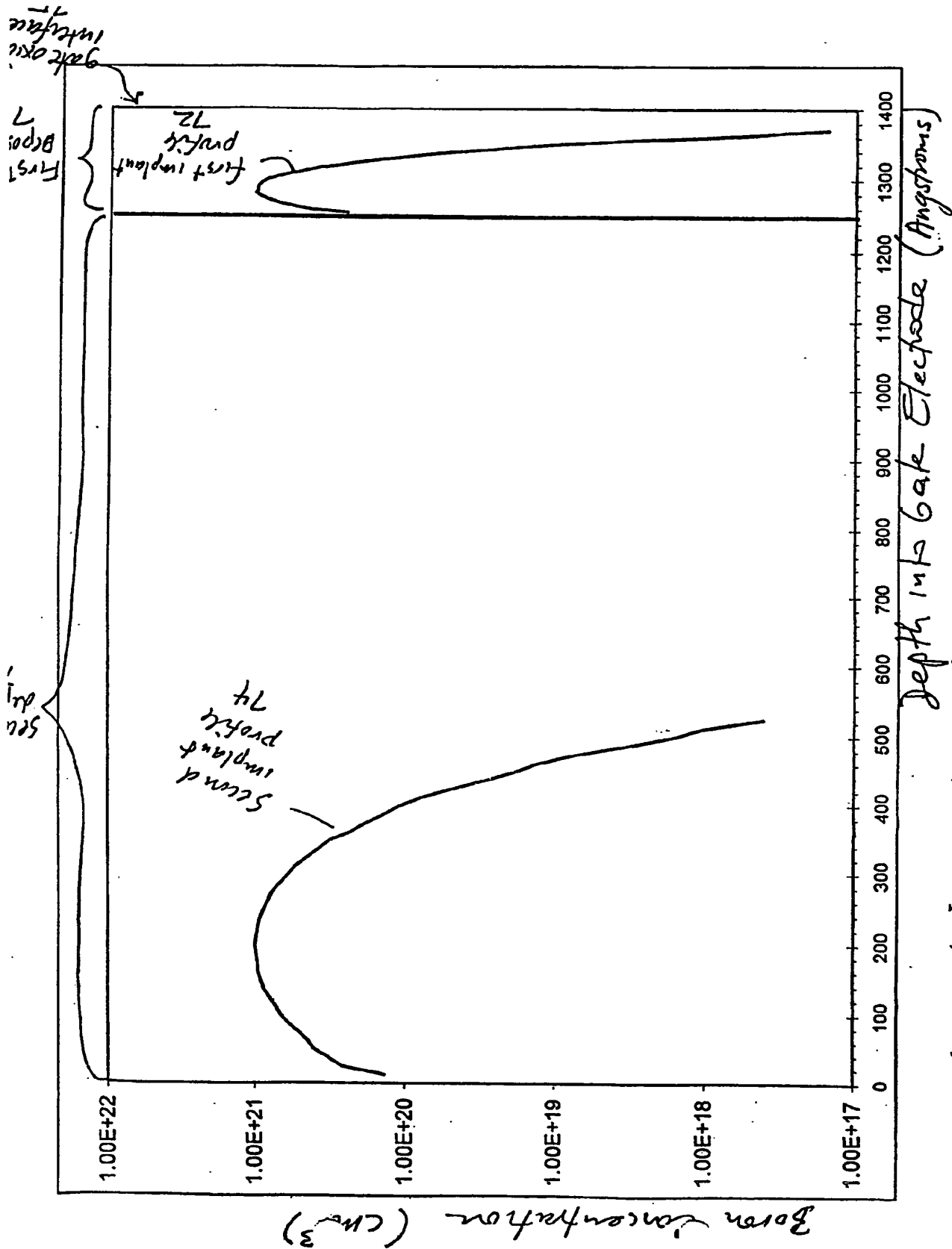


FIG 5 Simulation of implant profiles

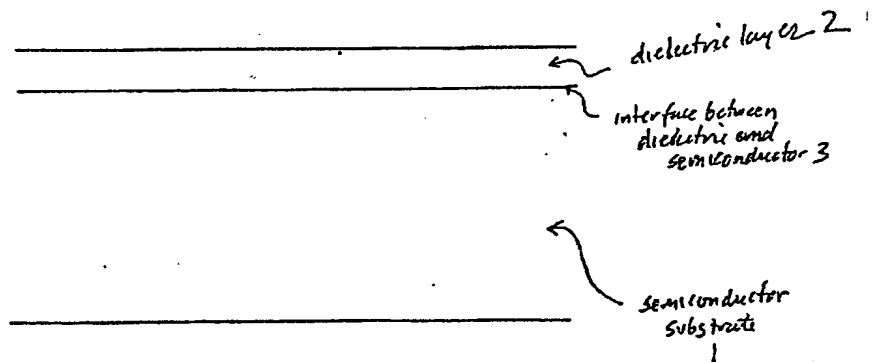


FIG 6 semiconductor substrate with dielectric layer on surface

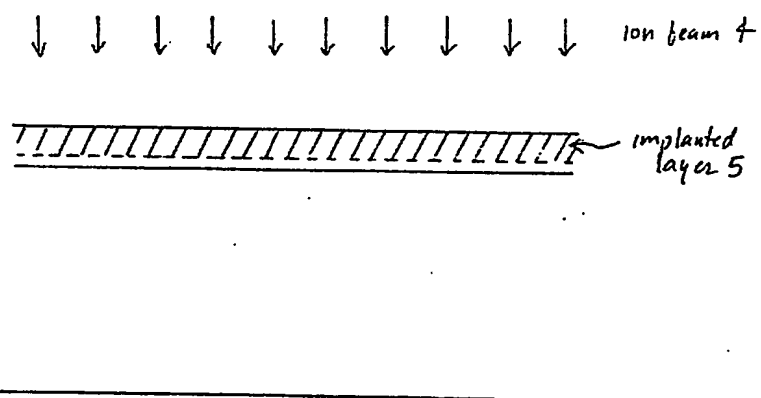
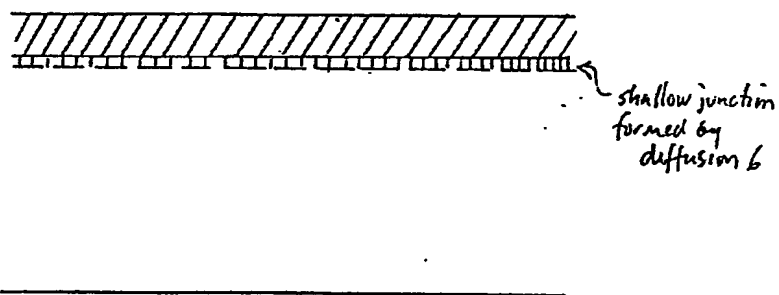


FIG. 7

: ion implant places dopant plus second species  
into implanted layer contained within dielectric



F168: After heat treatment, a shallow junction has been formed in the semiconductor substrate.